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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/697,315	10/31/2003	Yoshinori Shizuno	OHG 141	9863

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RABIN & Berdo, PC
1101 14TH STREET, NW
SUITE 500
WASHINGTON, DC 20005

EXAMINER	
ARORA, AJAY	

ART UNIT	PAPER NUMBER
2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,315	SHIZUNO, YOSHINORI	
	Examiner	Art Unit	
	AJAY K. ARORA	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10,11,13,14 and 16-23* is/are pending in the application.

4a) Of the above claim(s) *2-8,11,13 and 14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1,10 and 16-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/14/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 16, 18, 19 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa (US 4,418,284), hereinafter Ogawa, in view of Paek (US 6,740,950), hereinafter Paek, and further in view of Yamaji (US 6,159,837), hereinafter Yamaji.

Regarding claim 1, Ogawa (refer to Figure 3) teaches a semiconductor device comprising:

a semiconductor chip (15);

first pads (6) provided on a main surface of said semiconductor chip;

a light-receiving element (Col. 4, line 33-35) portion (3) provided on said main surface of said semiconductor chip such that a light-receiving surface (3) thereof is exposed;

a light-transmitting portion (7) provided so as to cover the light-receiving surface (3) of said light-receiving element portion for transmitting incoming light to said light-receiving element portion;

an insulating film (13) provided over said main surface of said semiconductor chip so as to expose surface portions of said first pads (6);

wiring patterns (wiring part of layer 5 that connects to pads 6) electrically connected to said first pads (6).

However, Figure 3 of Ogawa does not show interconnection details of the first pads (6) to form external terminals, and as such, does not teach the claimed interconnection details like, the wiring patterns "extending from said surface portions of said first pad and over said insulating film"; the "post portions", the "sealing layer" and the "external terminals".

Paek (refer to Figure 7) teaches a semiconductor device comprising a light-receiving element portion (550) and a sealing layer (560), such that sealing layer is provided on a side surface of said light-transmitting portion (550) and such that an upper surface of said light-transmitting portion is exposed. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa to incorporate the teachings of Paek such that the sealing layer is provided on a side surface of said light-transmitting portion and such that an upper surface of said light-transmitting portion is exposed. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of protecting the semiconductor die from external

environment by covering the active side with the sealing layer (see Paek, Col. 12, lines 26-29) while still preserving the light-transmitting functionality by keeping an upper surface of said light-transmitting portion exposed.

Further, Yamaji (refer to Figure 4) teaches a semiconductor device with a semiconductor chip (1), first pads (2) with surface portions, wiring patterns (4) and insulating film (3), wherein:

the wiring patterns (4) extend from said surface portions of said first pads and over said insulating film

post portions (7) provided on said wiring patterns (4);

a sealing layer (5) provided on a side surface of said light-transmitting portion (this would follow if the first pads 6 of Figure 3 of Ogawa are modified in view of first pads 2 of Figure 4 of Yamaji and Yamaji's corresponding interconnection details as explained above) and on side surfaces of said post portions (7), such that an upper surface of said light-transmitting portion is exposed (in view of the teaching of Paek explained above) and top surfaces of post portions are exposed, said sealing layer having sides surfaces which are substantially in the same plane of side surfaces of said semiconductor chip (1); and

external terminals (8) provided on the top surfaces of said post portions (7).

It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa to incorporate the teachings of Yamaji as explained above. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of

creating a flip chip mounted package with mounting bumps on the side of the chip with the chip pads, utilizing the post portions to provide the required height of the interconnects.

It is to be noted that claim 1 is a product claim, but recites "cut side surfaces which are cut by a blade", which is a method or process step. As such, claim 1 is a product-by-process claim. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113.

Regarding claim 16, Ogawa (refer to Figure 3) teaches a semiconductor device comprising:

a semiconductor chip (15) having a first main surface and a second main surface opposed to the first main surface;

a first pad (6) formed on the first main surface;

a light-receiving (Col. 4, line 33-35) element (3) formed on the first main surface;

a light-transmitting member (7) provided over said light-receiving element (3), said light transmitting member transmitting incoming light to said light-receiving element;

an insulating film (13) provided over said first main surface, so as to expose surface portions of said first pads (6);

a wiring pattern (wiring part of layer 5 that connects to pads 6) electrically connected to said first pads (6).

However, Figure 3 of Ogawa does not show interconnection details of the first pads (6) to form external terminals, and as such, does not teach interconnection details like the wiring patterns "extending from said surface portions of said first pad and over said insulating film"; the "post electrode", the "sealing layer" and the "external terminals".

Paek (refer to Figure 7) teaches a semiconductor device comprising a light-receiving element member (550) and a sealing layer (560), such that sealing layer is provided on a side surface of said light-transmitting member (550) and such that an upper surface of said light-transmitting member is exposed. It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa to incorporate the teachings of Paek so that the sealing layer is provided on a side surface of said light-transmitting member and such that an upper surface of said light-transmitting member is exposed. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of protecting the semiconductor die from external environment by covering the active side with the sealing layer (see Paek, Col. 12, lines

26-29) while still preserving the light-transmitting functionality by keeping an upper surface of said light-transmitting member exposed.

Further, Yamaji (refer to Figure 4) teaches a semiconductor device with a semiconductor chip (1), first pads (2) with surface portions, wiring patterns (4) and insulating film (3), wherein:

the wiring pattern (4) extends from said surface portions of said first pad and over said insulating film;

a post electrode (7) formed on the wiring pattern (4);

a sealing layer (5) formed on a side surface of said light-transmitting member (this would follow if the first pad 6 of Figure 3 of Ogawa are modified in view of first pad 2 of Figure 4 of Yamaji and Yamaji's corresponding interconnection details as explained above) and on side surfaces of said post electrode (7), such that an upper surface of said light-transmitting member is exposed (in view of the teaching of Paek explained above) and a top surface of said post electrode are exposed, said sealing layer having sides surfaces which are substantially in the same plane of side surfaces of said semiconductor chip (1); and

external terminals (8) formed on a top surface of said post electrode (7).

It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa to incorporate the teachings of Yamaji as explained above. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of

creating a flip chip mounted package with mounting bumps on the side of the chip with the chip pads, utilizing the post electrode to provide the required height of the interconnects.

It is to be noted that claim 16 is a product claim, but recites "cut side surfaces which are cut by a blade", which is a method or process step. As such, claim 1 is a product-by-process claim. Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985), MPEP 2113.

Regarding claims 18 and 19, if Ogawa is modified in view of Paek and Yamaji as above, the sealing layer (560 of Figure 7 of Paek) will directly contact the side surfaces of said light-transmitting member or light-transmitting portion (550 of Figure 7 of Paek).

Regarding claims 20 and 22, if Ogawa is modified in view of Paek and Yamaji as above, the said wiring patterns (4 of Figure 4 of Yamaji) physically and directly contact said surface portions of said first pad (2 of Figure 4 of Yamaji).

Regarding claims 21 and 23, if Ogawa is modified in view of Paek and Yamaji as above, the said wiring patterns (4 of Figure 4 of Yamaji) are uniformly spaced apart from said first main surface of said semiconductor chip (1 of Figure 4 of Yamaji).

2. Claims 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogawa, Paek and Yamaji as applied to claims 1 and 16 above, and further in view of Lanford (US 5,959,358), hereinafter Lanford.

Regarding claims 10 and 17, Ogawa as modified above teaches substantially the claimed semiconductor device but does not teach that "an oxidation film" is formed on the side surface of said post portions or post electrodes. Lanford teaches copper interconnects or wiring for microelectronic devices, wherein an oxidation film is formed on side surfaces of the interconnects/wiring (Col. 4, lines 1-9). It would have been obvious to one of ordinary skills in the art at the time of the invention to modify Ogawa so that an oxidation film is formed on the side surface of said post portions. The ordinary artisan would have been motivated to modify Ogawa for at least the purpose of creating an inert protective layer that prevents further oxidation of the post portions (Col. 4, lines 1-9).

Response to Arguments

3. Applicant's arguments of 02/12/2008 with respect to amended claims 1 and 16, and their dependent claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AJAY K. ARORA whose telephone number is (571)272-8347. The examiner can normally be reached on Mon through Fri, 8am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571) 272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/A. K. A./
Examiner, Art Unit 2892

/Thao X Le/
Supervisory Patent Examiner, Art Unit 2892